EE - 4173

Computer System Engineering & Performance

Curricular Designation: EE: elective     CpE: required

Catalog Description:

EE 4173 - Computer System Engineering & Performance. Covers the principles and practices of modern computer architecture. Emphasizes quantitative performance evaluation of: memory hierarchies, from cache through virtual memory; pipelined processors with advanced hazard management; and combined processor/memory systems. Introduces RAID, superscalars, parallel processing, cache coherence, performance simulation software. Credits: 3.0, Lec-Rec-Lab: (3-0-0), Semesters Offered: Fall, Spring, Restrictions: Must be enrolled in one of the following Major(s): Computer Engineering, Pre-Requisite(s): CS 3421 and EE 3173.

Textbooks(s) and/or Other Required Materials:

2. Relevant manuals for COTS software tools used in the course.
3. Articles & data sheets from the technical literature – to supplement or update textbook material.

Prerequisites by Topic:

1. Familiarity with basic combinatorial probability, incl: conditional probabilities.
2. Familiarity with digital logic design, digital electronics, pipeline organization, assembly level processor organization, one assembler language, and one high-level language.
3. Familiarity with hierarchical memory system components, incl: cache organizations, and the technologies, organization & signaling conventions for SRAM, DRAM, & FLASH devices.

Course Objectives 1:

1. Understand the factors that contribute to computer performance & drive decisions about alternative approaches & trade-offs. Master both the basic principles, & the complexity of existing commercial systems. Understand the effect on system performance of changes to functional units.
2. Master the concepts of memory hierarchy & cost-performance trade-offs, incl: the operation of different kinds of storage (SRAM, DRAM, DDR, magnetic disks (HDDs) & SSDs); the effect of memory latency & bandwidth on performance; principles of memory management; virtual memory realization in hardware; trade-offs in terms of mem size (main mem, cache mem, auxiliary mem).
3. Develop a practical understanding of CPU design & organization; its integration into the computer system, & how various peripheral devices interact with CPU; CISC & RISC ISAs; principles of pipelining; ILP; the major hazards & advanced hazard resolution methods; overcoming the effect of branches & memory latency; how ISAs have evolved to improve performance.
4. Introduction to RAID, superscalar architecture, dynamic scheduling, parallel processing.
5. Familiarity with Performance metrics; the main models used to evaluate a system; the role of modeling & simulation in system design; derivation of analytical models; the ability to integrate analytic & simulation models to evaluate system-wide performance & design trade-offs.

Topics Covered ¹:

1. Memory system hierarchy: organization; architecture; visualization models & derivation of N-Layer mean access time; impact of locality & inclusion; integration of analytic & simulation models.
   (a) Physical memory technologies: SRAM, DRAM, DDR, EPROM, FLASH, Magnetic.
   (b) Cache memories: address mapping; line size; placement, replacement, & write-back policies; working sets; hit & miss times vs. organization; design trade-offs vs. the 3 causes of misses.
   (c) Main memory: organization & performance; latency; cycle time; bandwidth; interleaving.
   (d) Virtual memory: organization & structure of disk drives & SSDs; memory management hardware; paging; placement & replacement policies; integrated whole-system modeling.

2. Instruction Pipelining: performance issues & options; quantitative performance analysis & evaluation; design trade-offs; Amdahl’s law.
   (a) CISC & RISC ISAs; derivation of the Pipeline Production Equation; pipeline hazards (structural, data & control); instruction-level parallelism (ILP); Superscalar architecture.
   (b) Reducing the effects of hazards (predecoding, prefetching, instruction buffering, reservation stations, data forwarding, register renaming, ROBs, Tomasulo’s algorithm, branch prediction, penalty mitigation, speculative execution); performance metrics (clock rate, MIPS, CPI); properties of benchmarks. Representative case studies, from the MIPS, ARM & x86 families.

3. Advanced topics: RAID; parallel machine models; Flynn’s taxonomy; VLIW; Vector & Array processors; multi-processors; multi-computers; multi-cores; multi-threading; & cache coherence.

Relationship of the Course Content to Program Outcomes:

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<tr>
<th>Outcome</th>
<th>Topics and Level of Coverage</th>
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<tbody>
<tr>
<td>an ability to apply knowledge of mathematics, science and engineering</td>
<td>Important</td>
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<td>an ability to design and conduct experiments, as well as to analyze and interpret data</td>
<td>Moderately Important</td>
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<tr>
<td>the ability to design a system, component, or process to meet desired needs within realistic constraints such as...</td>
<td>Minimally Important</td>
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<tr>
<td>an ability to function on multi-disciplinary teams</td>
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<td>an ability to identify, formulate and solve engineering problems</td>
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<td>an understanding of professional and ethical responsibility</td>
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<td>an ability to communicate effectively</td>
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<td>the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental and societal context</td>
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<td>recognition of the need for, and an ability to engage in life-long learning</td>
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<tr>
<td>a knowledge of contemporary issues</td>
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<td>the ability to use the techniques, skills, and modern engineering tools necessary for the practice of computer engineering</td>
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Contribution of Course to Meeting Degree Requirements: 3 Credit Hrs - Engineering Topics
Class/Laboratory Schedule: Lecture: 40 hours = 3 hrs/wk for 13.33 weeks (1 hr = 50 mins):