

## STEVEN M. CARR

Department of Computer Science  
Michigan Technological University  
Houghton MI 49931  
Ph: (906) 487-2958  
*carr@mtu.edu*

### RESEARCH INTERESTS

Dynamic program analysis, program locality analysis, PGAS language optimization, high-performance computing, memory-hierarchy optimizations, language run-time systems, virtualization, code generation for embedded systems, cooperation between architecture and compilers.

### EDUCATION

Ph.D., Rice University, 1993 (Computer Science)  
**Thesis Title:** Memory-hierarchy Management  
**Adviser:** Ken Kennedy  
M.S., Rice University, 1990 (Computer Science)  
B.S., Michigan Technological University, 1987 (Computer Science)

### EMPLOYMENT

#### Michigan Technological University, Department of Computer Science

*Chair:* July 2011 - present  
*Interim Chair:* July 2010 – June 2011  
*Professor:* August 2004 – present  
*Associate Professor:* September 1999 – August 2004  
*Assistant Professor:* August 1993 – August 1999

*Courses Taught:* introduction to programming II, discrete mathematics, data structures, numerical methods, introduction to computation theory, programming languages, computer and network security, parallel programming, compiler construction, compiler optimization, and high-level program analysis and optimization.

#### Rice University, Department of Computer Science

*Research Scientist:* October 1992 to July 1993

### GRANTS

1. “Compiler Evaluation for the PowerPC 476 Processor”, LSI Corporation, co-PIs: Steve Carr and Zhenlin Wang, 5/10 – 8/10, \$18,215.
2. “Feedback-Directed Resource Management in Virtual Private Machines”, National Science Foundation, co-PIs: Steve Carr and Zhenlin Wang, 9/08 – 12/10, \$60,000.

3. "A Performance Model for Partitioned Global Address Space Languages", National Science Foundation, PI: Steven R. Seidel, co-PIs: Steve Carr and Zhenlin Wang, 9/08 – 8/10, \$70,000.
4. "Compiler Development for the Agere Payload Plus Network Processor", Agere Systems, PI, 9/04 - 12/05, \$85,267.
5. "ITR: Exposing the Compiler to the Hardware: Memory Subsystem Optimizations through Compiler/Micro-architecture Cooperation using Set Membership Information and Color Sets", National Science Foundation, PI: Soner Önder, co-PI: Steve Carr, 9/03 - 8/06, \$280,000.
6. "Compilation for the Agere APP5xx and APP7xx Family of Network Processors", Agere Systems, PI, 1/03 - 12/03, \$62,068.
7. "High-Level Optimization for DSP Architectures" National Science Foundation, PI, 9/02 - 8/05, \$249,964.
8. "Concurrent Computing in an Upper-Level Computer Science Curriculum", National Science Foundation, PI, co-PIs: Jean Mayo and C.-K. Shene, 6/00 - 5/03, \$299,865.
9. "Code Generation for ILP Architectures with Partitioned Register Files", National Science Foundation, PI: Philip H. Sweany, co-PI: Steve Carr, 7/98 - 6/02, \$325,434.
10. "Teaching Multithreaded Programming to Computer Science Undergraduates", National Science Foundation, PI: C.K. Shene, co-PI: Steve Carr, 3/98 - 5/99, \$50,002.
11. "Register-Bank Assignment for Distributed-Register, Instruction-Level Parallel Architectures", Texas Instruments, PI: Philip H. Sweany, co-PI: Steve Carr, 9/97 - 8/98, \$42,830.
12. "Generating Efficient Code for Horizontal Micro-Architectures with Partitioned Register Files", Texas Instruments, PI: Philip H. Sweany, co-PI: Steve Carr, 9/95-8/96, \$23,715.
13. "Hiding the Latency Between Level-1 and Level-2 Cache on the DEC Alpha 21164", Digital Equipment Corporation, PI, co-PI: Philip H. Sweany, 7/95-8/97, \$137,647.
14. "Improving Memory Performance on the Hewlett-Packard PA-RISC", Hewlett-Packard Company, PI, 9/94-8/95, \$53,480.
15. "Improving the Cache Performance of Scientific Applications", National Science Foundation, PI, 7/94-6/97, \$90,984.
16. "Cache-Conscious Loop Unrolling", Hewlett-Packard Company, PI, 7/93, \$41,984.

## **PENDING PROPOSALS**

1. "Predictive and Adaptive Memory Resource Management in a Virtualized System", National Science Foundation, PI: Zhenlin Wang, co-PI: Steve Carr, \$483,079.
2. "Investigation into the Parallel Architecture for the Efficient Implementation of Multi View Video Coding", National Science Foundation, PI: Saeid Nooshabadi, co-PIs: Steve Carr, Zhenlin Wang and Soner Önder, \$499,957.

## JOURNAL PUBLICATIONS

1. J. Mayo and S. Carr. "Teaching Access Control with Domain Type Enforcement", To appear in *The Journal of Computing in Small Colleges*.
2. S. Carr and P. Sweany. "An Experimental Evaluation of Scalar Replacement on Scientific Benchmarks", *Software - Practice & Experience* 33(15), December 2003.
3. S. Carr, J. Mayo and C.-K. Shene. "ThreadMentor: A Pedagogical Tool for Multithreaded Programming", *ACM Journal of Educational Resources in Computing* 3(1), March 2003.
4. S. Carr, J. Mayo and C.-K. Shene. "Race Conditions: A Case Study", *The Journal of Computing in Small Colleges* 17(1), September 2001.
5. P. Sweany, S. Carr and B.L. Huber, "Global Instruction Scheduling Without Copies", *Digital Technical Journal* 10(1), December 1998.
6. C.-K. Shene and S. Carr. "The Design of a Multithreaded Programming Course and Its Accompanying Software Tools", *The Journal of Computing in Small Colleges* 14(1), November 1998.
7. S. Carr and R.B. Lehoucq, "Compiler Blockability of Dense Matrix Factorizations", *ACM Transactions on Mathematical Software* 23(3), September 1997.
8. K. McKinley, S. Carr and C.-W. Tseng, "Improving Data Locality with Loop Transformations", *ACM Transactions on Programming Languages and Systems* 18(4), July 1996.
9. S. Carr and K. Kennedy, "Improving the Ratio of Memory Operations to Floating-Point Operations in Loops", *ACM Transactions on Programming Languages and Systems* 16(6), November 1994.
10. S. Carr and K. Kennedy, "Scalar Replacement in the Presence of Conditional Control Flow", *Software - Practice & Experience* 24(1), January 1994.

## REFEREED CONFERENCE PUBLICATIONS

1. C. Fang, S. Carr, S. Onder and Z. Wang. "Feedback-directed Memory Disambiguation Through Store Distance Analysis", In *Proceedings of the 20th ACM International Conference on Supercomputing*, Queensland, Australia, June 2006.
2. C. Fang, S. Carr, S. Onder and Z. Wang. "Path-based Reuse Distance Analysis", In *Proceedings of the 15th International Conference on Compiler Construction*, Vienna, Austria, March 2006.
3. C. Fang, S. Carr, S. Onder and Z. Wang. "Instruction Based Memory Distance Analysis and Its Application to Optimization", In *Proceedings of the Fourteenth ACM/IEEE International Conference on Parallel Architectures and Compilation Techniques*, St. Louis, MO, September 2005.

4. P. Zhou, S. Onder and S. Carr. "Fast Branch Misprediction Recovery in Out-of-order Superscalar Processors", In *Proceedings of the 2005 ACM International Conference on Supercomputing*, Boston, MA, June 2005.
5. S. Carr and S. Onder. "A Case for a Working-set-based Memory Hierarchy", In *Proceedings of the 2005 ACM International Conference on Computing Frontiers*, Ischia, Italy, May 2005.
6. S. Carr and P. Sweany. "Automatic Data Partitioning for the Agere Payload Plus Network Processor", In *Proceedings of the ACM/IEEE 2004 International Conference on Compilers, Architecture and Synthesis for Embedded Systems*, Washington, D.C., September 2004.
7. Y. Ma, S. Carr and R. Ge. "Low-cost Register-pressure Prediction for Scalar Replacement Using Pseudo-schedules", In *Proceedings of the 2004 International Conference on Parallel Processing*, Montreal, Quebec, August 2004.
8. C. Fang, S. Carr, S. Onder and Z. Wang. "Reused-distance-based Miss-rate Prediction on a Per Instruction Basis", In *Proceedings of the 2004 ACM Workshop on Memory System Performance*, June 2004.
9. S. Carr, C. Fang, T. Jozwowski, J. Mayo and C.-K. Shene. "ConcurrentMentor: A Visualization System for Distributed Programming Education". In *Proceedings of the 2003 International Conference on Parallel and Distributed Processing Techniques and Applications*, Las Vegas, NV, June 2003.
10. Y. Qian, S. Carr and P. Sweany. "Optimizing Loop Performance for Clustered VLIW Architectures", In *Proceedings of the Eleventh IEEE International Conference on Parallel Architectures and Compiler Techniques (PACT-2002)*, Charlottesville, Virginia, September 22-25, 2002.
11. Y. Qian, S. Carr and P. Sweany. "Loop Fusion for Clustered VLIW Architectures", In *Proceedings of the ACM 2002 Joint Conference on Languages, Compilers and Tools for Embedded Systems/Software and Compilers for Embedded Systems*, Berlin, Germany, June 2002.
12. S. Carr, P. Chen, T. Jozwowski, J. Mayo and C.-K. Shene. "Channels, Visualization and Topology Editor", In *Proceedings of the Seventh Annual ACM SIGCSE Conference on Innovation and Technology in Computer Science Education*, Aarhus, Denmark, June 2002.
13. D. Sule, S. Carr, and P. Sweany. "Evaluating Register Partitioning with Genetic Algorithms", In *Proceedings of the Fourth International Conference on Massively Parallel Computing Systems*, Ischia, Italy, April 2002.
14. S. Carr, C. Fang, T. Jozwowski, J. Mayo and C.-K. Shene. "A Communication Library to Support Concurrent Programming Courses", In *Proceedings of the 33rd ACM SIGCSE Technical Symposium on Computer Science Education*, Northern Kentucky, February 2002.
15. X. Huang, S. Carr and P. Sweany. "Loop Transformations for Architectures with Partitioned Register Banks", In *Proceedings of the 2001 Workshop on Languages, Compilers and Tools for Embedded Systems (LCTES '2001)*, Snowbird, Utah, June 22-23, 2001.

16. M. Bedy, S. Carr, S. Onder and P. Sweany. "Improving Software Pipelining by Hiding Memory Latency with Combined Loads and Prefetches", In *Interaction between Compilers and Computer Architectures*, G. Lee and P.-C. Yew ed., Kluwer Academic Publishers, 2001.
17. J. Hiser, S. Carr and P. Sweany. "Global Register Partitioning", In *Proceedings of the 2000 International Conference on Parallel Architectures and Compiler Techniques*, Philadelphia, PA, October 15-19, 2000.
18. S. Carr and C.-K. Shene. "A Portable Class Library for Teaching Multithreaded Programming". In *Proceedings of the Fifth Annual Conference on Innovation and Technology in Computer Science Education*, Helsinki, Finland, July 11-13, 2000.
19. J. Hiser, S. Carr, P. Sweany, and S.J. Beaty. "Register Assignment for Software Pipelining with Partitioned Register Banks". In *Proceedings of the 2000 International Parallel and Distributed Processing Symposium*, Cancun, Mexico, May 1-4, 2000.
20. M.J. Bedy, S. Carr, X. Huang and C.-K. Shene. "A Visualization System for Multithreaded Programming", In *Proceedings of the 31st Annual SIGCSE Technical Symposium on Computer Science Education*, Austin, TX, March 8-12, 2000.
21. M.J. Bedy, S. Carr, X. Huang and C.-K. Shene. "The Design and Construction of a User-Level Kernel for Teaching Multithreaded Programming", In *Proceedings of the 1999 ASEE/IEEE Frontiers in Education*, San Juan, Puerto Rico, November 10-13, 1999.
22. S. Jang, S. Carr, P. Sweany, and D. Kuras, "A Code Generation Framework for VLIW Architectures with Partitioned Register Files". In *Proceedings of the Third International Conference on Massively Parallel Computing Systems*, Colorado Springs, Colorado, April 1998.
23. S. Carr and Y. Guan. "Unroll-and-Jam Using Uniformly Generated Sets", In *Proceedings of the 30th International Symposium on Microarchitecture (MICRO-30)*, Research Triangle Park NC, December 1997.
24. C. Ding, S. Carr, and P. Sweany. "Modulo Scheduling with Cache-Reuse Information", *Lecture Notes in Computer Science 1300*, Springer-Verlag, Proceedings of Europar 97, Passau, Germany, August 1997.
25. S. Carr. "Combining Optimization for Cache and Instruction-Level Parallelism", In *Proceedings of the 1996 International Conference on Parallel Architectures and Compiler Techniques (PACT 96)*, Boston MA, October 1996.
26. S. Carr, C. Ding and P. Sweany, "Improving Software Pipelining with Unroll-and-Jam", In *Proceedings of the Twenty-Ninth Annual Hawaii International Conference on System Sciences*, Maui HI, January 1996.
27. T. Brasier, P. Sweany, S. Beaty and S. Carr, "CRAIG: A Practical Framework for Combining Instruction Scheduling and Register Assignment", In *Proceedings of the 1995 International Conference on Parallel Architectures and Compilation Techniques (PACT 95)*, Cyprus, June 1995.

28. S. Carr and R.B. Lehoucq, "A Compiler Blockable Algorithm for QR Decomposition", In *Proceedings of the 7th SIAM Conference on Parallel Processing for Scientific Computing*, San Francisco CA, February 1995.
29. S. Carr, K.S. McKinley and C-W. Tseng, "Compiler Optimizations for Improving Data Locality", In *Proceedings of the Sixth International Conference on Architectural Support for Programming Languages and Compilers (ASPLOS-VI)*, San Jose CA, October 1994.
30. S. Carr and K. Kennedy, "Compiler Blockability of Numerical Algorithms", In *Proceedings of Supercomputing '92*, Minneapolis MN, November 1992.
31. S. Carr, D. Callahan and K. Kennedy, "Improving Register Allocation for Subscripted Variables", In *Proceedings of the ACM SIGPLAN 1990 Conference on Programming Language Design and Implementation (PLDI 90)*, White Plains NY, June 1990.

## REFEREED WORKSHOP PUBLICATIONS

1. S. Vormwald, W. Wang, S. Carr, S. Seidel and Z. Wang. "Predicting Remote Reuse Distance Patterns in UPC Applications", In *PGAS 10: Proceedings of the Fourth Conference on Partitioned Global Address Space Programming Models* (Workshop), October, 2010 (to appear).
2. Y. Ma and S. Carr. "Register Pressure Guided Unroll-and-Jam", In *The 2008 Open64 Workshop*, Boston, MA, April 6, 2008.
3. P. Sweany and S. Carr. "Building a C Compiler Retargetable for DSP Processors", In *Proceedings of the 1<sup>st</sup> Workshop on Optimizations for DSP and Embedded Systems*, San Francisco, CA, March 2003.
4. D. Kuras, S. Carr and P. Sweany. "Value Cloning for Architectures with Partitioned Register Banks", In *The 1998 Workshop on Compiler Support for Embedded Systems (CASES98)*, Washington D.C., December 1998.
5. S. Carr and P. Sweany. "Improving Software Pipelining with Hardware Support for Self-Spatial Loads", In *Proceedings of the Third Workshop on Interaction between Compilers and Computer Architecture (INTERACT-3)*, San Jose, CA, October 1998.

## INVITED PUBLICATIONS

1. D. Callahan, S. Carr and K. Kennedy. "Retrospective: Improving Register Allocation for Subscripted Variables", In *20 Years of the ACM Conference on Programming Language Design and Implementation (1979 - 1999): A Selection*.
2. S. Carr and K. Kennedy, "Compiling Scientific Code for Complex Memory Hierarchies", In *Proceedings of the Twenty-Fourth Annual Hawaii International Conference on System Sciences*, Kauai HI, January 1991.
3. S. Carr and K. Kennedy, "Blocking Linear Algebra Codes for Memory Hierarchies", In *Proceedings of the Fourth SIAM Conference on Parallel Processing for Scientific Computing*, Chicago IL, December 1989.

## PAPER SUBMISSIONS

1. W. Wang, S. Carr, S. Seidel and Z. Wang. “Application Specific Software Cache Design for PGAS Applications”, To be submitted to Supercomputing ’11.
2. W. Wang, S. Carr, S. Seidel and Z. Wang. “Software Cache Prefetching in a PGAS Run-time System”, To be submitted to Languages and Compilers for Parallel Computing 2011.
3. D. Larson, S. Carr and Z. Wang. “A Performance Analysis of JIT Compiler Optimization”, under preparation.
4. J. Slepak, S. Carr and Z. Wang. “On-the-fly Reuse Distance Prediction using Performance Monitors”, under preparation.

## PROFESSIONAL ACTIVITIES

### Conference Program Committee Memberships:

ACM SIGMICRO MICRO-29, Paris, France, December 1996.

ACM SIGPLAN PLDI 97, Las Vegas NV, June 1997.

Euromicro MPCS 98, Colorado Springs, CO, April 1998

Euromicro MPCS 02, Ischia, Italy, April 2002

ACM PACT 2003, New Orleans, LA, September 2003.

ACM PACT 2005, St. Louis, MO, September 2005.

ACM PACT 2008, Toronto, Ontario, Canada, October 2008.

ACM MSP 2005, Chicago, IL, June 2005.

ACM Computing Frontiers 2005, Ischia, Italy, May 2005.

### Conference Organizing Committee Memberships:

ACM PACT 2002, Charlottesville, VA, September 2002.

## SERVICE

Graduate Faculty Council 2000-02 (Secretary 2000-01)

University Senate, 1998-2000, 2001-02

Undergraduate adviser, 2000 – 2009

Advised or co-Advised 3 PhD Dissertations and 14 MS Theses

Currently co-advising 1 PhD Dissertation and 1 MS Thesis

Advised 3 undergraduate research projects

Graduate Program Director, 1996-2003, 2006-2010

University Academic Integrity Committee, 2005-08

College of Sciences & Arts Promotion and Tenure Committee, 2006-09 (Chair 2007-09)

University Committee on Academic Tenure, Promotion and Reappointment, 2009 – 2010